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This overview summarizes the major functions performed by the **UNIX**™ PC Ethernet Expansion Board hardware. The topics covered here include:

- Interface I/O description
- Status and command circuitry
- State machine control circuitry
- LANCE interface
- Ethernet interface
- Software interface

Ethernet Expansion Board

The Ethernet Expansion Board (EEB), when plugged into an AT&T **UNIX**™ PC, provides an interface to an Ethernet communications network operating at a transfer rate of 10MB/sec. The EEB is based on the AMD 7990 and 7992 chip set, which performs the following functions:

- AM7990 Local Area Network Controller for Ethernet (LANCE) performs memory management, packet handling, error reporting, and interface functions.
- AM7992 Serial Interface Adapter (SIA) performs Manchester encoding and decoding of the serial bit stream with phase lock loop, clock recovery.

The Expansion Board, as shown in the Figure 1 block diagram, is a circuit board containing the I/O and DMA interface to the LANCE chip, a state machine with a read/write control register, a separate DMA controller for LANCE status, and a board ID/Ethernet address ROM.

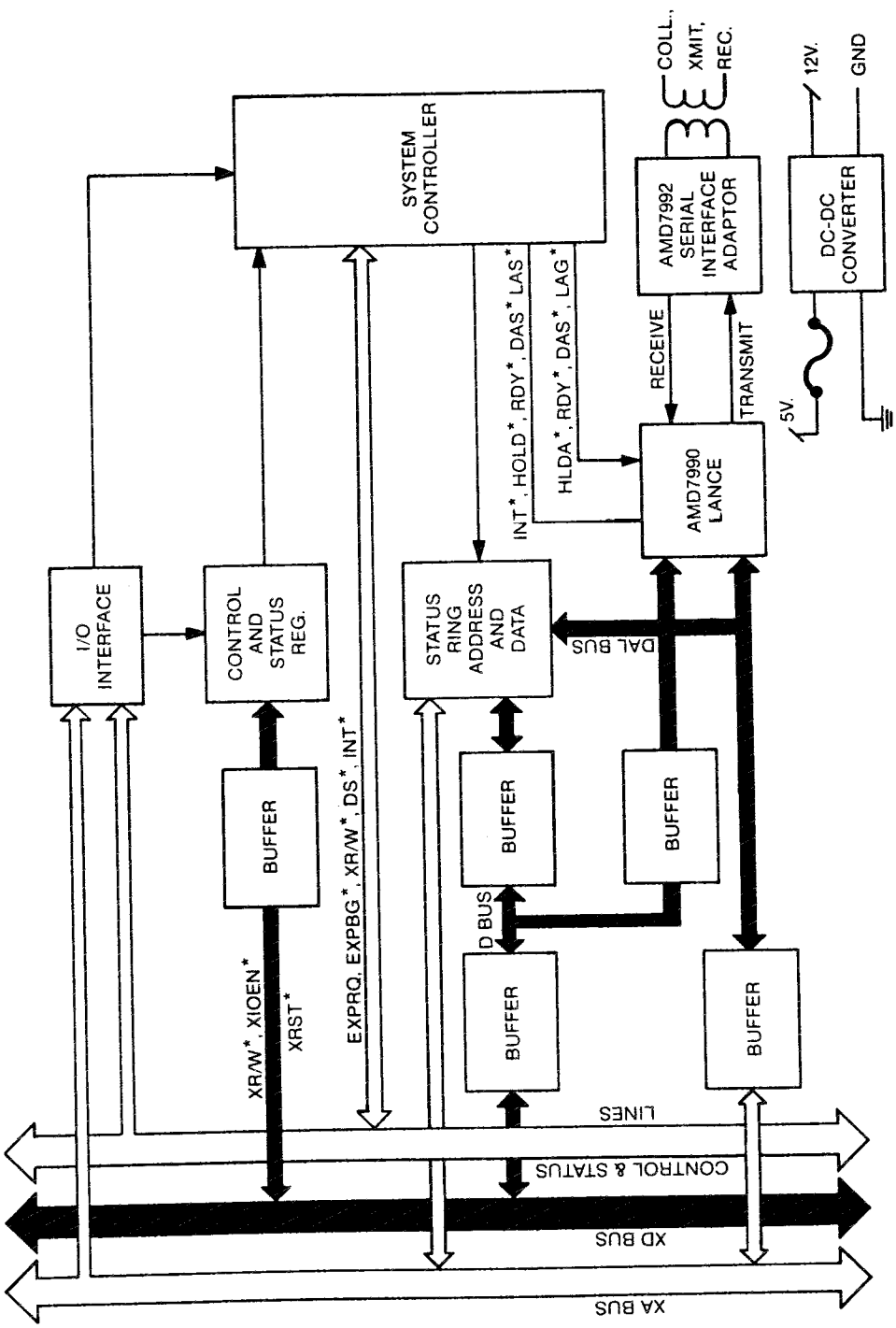


Figure 1 Expansion Board Block Diagram

Once the LANCE chip is initialized, all data transfers including buffer chaining are handled by the chip. Timing and control are maintained by the on-board state machine. LANCE status is transferred to memory by a separate state machine DMA controller on each LANCE interrupt. This status is placed in a 256-word ring in memory allowing the software a 256-packet interrupt latency. Because of maximum throughput, the CPU is able to find all data and status in memory and never needs to talk directly to the board. The board is also not required to wait for CPU response or to share board resources with the CPU accesses.

LANCE operation consists of two distinct modes, transmit and receive. In the transmit mode, the LANCE chip directly accesses data in memory. Data is conditioned by adding a preamble, sync pattern, and appending a 32-bit cycle redundancy check (CRC).

This packet is sent from the LANCE to the AM7992A Serial Interface Adapter (SIA). The SIA then transmits this packet to the Ethernet system AM7995 transceiver. In the receive mode, packets are sent by the SIA to the LANCE.

Ethernet Interface

The Ethernet system, to which the EEB is connected, consists of an external AM7995 transceiver with power supply and the Ethernet coax transmission line. The EEB is connected to this system by cable. For a detailed description of the Ethernet system interface, refer to the **Ethernet/IEEE 802.3** specification and the technical manual for **Local Area Network Controller AM 7990 (LANCE)** by Advanced Micro Devices.

Interface I/O Description

The expansion-board interface consists of drivers and receivers for all required signals to and from the **UNIX** PC's expansion bus. The expansion data bus goes through buffers that are controlled by the state machine section to create the internal data bus.

The address bus and the bus cycle control signals are received with buffers that are always enabled to create the internal address and control bus. The internal address and control bus, with the comparator for board ID, allows constant monitoring for board I/O requests, which are then passed on to the state machine.

For board-initiated DMA cycles, the state machine-generated request, read/write, and data strobe signals are also driven onto the expansion bus by this section.

Status and Command Circuitry

The amount of on-board status and command information is limited. The board ID function has been expanded to allow the CPU to interrogate the board for the 6-byte Ethernet address, as well as for the required 4-byte board ID. This information is contained in a 32-byte prom accessed at odd byte addresses in the upper 32 bytes of the board address block. A write to any of these addresses produces a board reset.

CPU Read/Write Access

The status and command section provides CPU read/write access to the LANCE chip address and data ports. However, due to the long access time of the chip, LANCE reads do not provide data to the CPU in a single cycle. Data is latched on board during the LANCE read; it is then read by the CPU in a separate latch read cycle.

LANCE Interrupt Status

This section contains a 16-bit register and an 8-bit counter. The LANCE interrupt status is written automatically to memory at the location of the combined 24-bit address by the on-board DMA.

Read/Write Control Register

A 4-bit read/write control register is also contained in this section. This register allows the CPU to disable DMA for diagnostic purposes, select Ethernet, and make selections between INT 01 and INT 05. The register contains one unused bit.

State Machine Control Circuitry

The state machine control section consists of five PALs providing control and timing signals for all other sections. A 20R8 PAL determines when a board cycle needs to be initiated and what type of cycle it should be. The 20R8 arbitrates between LANCE DMA requests (HOLD), LANCE interrupts, and CPU I/O requests and generates the LANCE HLDA and expansion bus requests as well as on-board I/O cycles.

Each of 11 non-idle cycles has its own timing and control requirements (see timing diagrams for more detail). These cycles consist of five CPU-initiated operations which are:

- CPU non-LANCE Read
- CPU non-LANCE Write
- CPU LANCE Read
- CPU LANCE Write
- CPU Data Latch Read

These are all individual cycles that can occur only when the state machine is in its idle state. The state machine is always returned to the idle state.

Three additional cycles are initiated by LANCE DMA requests. These are:

- request cycle
- LANCE DMA read cycle
- LANCE DMA write cycle

The request cycle precedes a single LANCE DMA cycle or burst of cycles. This cycle insures **UNIX** PC LANCE synchronization. The LANCE DMA read or write cycles follow the request cycle. The state machine goes directly from the request cycle to the read or write without going through idle. As long as the LANCE DMA request stays active, each DMA cycle leads directly to the next, again without idle. LANCE DMA requests are either single cycle for buffer management fetches or bursts of eight cycles for data transfers.

The three final cycle types are also linked together with no intervening idle states. When the LANCE asserts its interrupt the state machine executes a status LANCE read cycle reading the LANCE interrupt status into the on-board data latch. A status DMA cycle is executed to place the status in the status ring in memory. Finally, a status LANCE write is executed to clear the LANCE interrupt, and a CPU interrupt is generated at the same time.

The 20R8 PAL encodes the cycle type in 4 bits. These 4 bits are fed to three additional registered PALS. These signals combine with a 3-bit counter for timing within each cycle and, with several handshake signals from the LANCE, allowing these three PALS to generate all LANCE-related timing and control signals.

In addition, an I/O cycle signal is generated for on-board non-LANCE cycles. This signal goes to the fifth PAL. This PAL is a nonregistered PAL that generates timing and control for on-board I/O that is based on I/O cycle and address decodes.

LANCE Interface

The LANCE interface consists of a 16-bit, multiplexed address and data bus with associated handshake signals. The hardware provides three sets of 16-bit latches for address, read data, and write data. This section also includes a buffer for the upper 5 bits of address and a 4-bit data buffer. These buffers provide for the status write to clear the LANCE interrupt.

Ethernet Interface

The Ethernet interface is handled by the AMD chip set. The LANCE chip sends transmit data to the 7992 and gets receive data and collision detection from the 7992. The 7992 provides the interface to the off-board transceiver through a standard 15-pin D-connector interface. Table 1 lists the pin-out assignments for this connector.

Table 1 Ethernet 15-Pin D Connector

Pin	Signal	Pin	Signal	Pin	Signal
1	GND	6	GND	11	Not Used
2	COL+	7	Not Used	12	RCVR-
3	TRANS+	8	Not Used	13	PLUS12
4	Not Used	9	COL-	14	Not Used
5	RCVR+	10	TRANS-	15	Not Used

Software Interface

The EEB occupies the standard 256Kbyte (or 128K word) block assigned to each expansion slot.

Expansion Slot

The expansion cards in the **UNIX** PC are each assigned 256K bytes of address space. Since all addressing is done on word boundaries, 128K words of address space is available. Expansion bus address bits XA1 - XA17 define this space. Each expansion slot contains hardwired identification bits XID0 - XID2 to define seven unique slot addresses. Bits XA18 - XA20 are compared against the slot identification bits to validate the address. Also, address bit XA21 is always zero; similarly, expansion addresses XA22 and XA23 are always ones.

Therefore, once the EEB is plugged into its slot, the predetermined XA18 - XA23 bits generate the offset address, while bits XA1 - XA17 are the base addresses used to access I/O devices.

The offset addresses used in the **UNIX** PC are listed below.

Table 2 Expansion Slot Offset Addresses

Slot Number	Offset Address (h)
0	0C00000
1	0C40000
2	0C80000
3	0CC0000
4	0D00000
5	0D40000
6	0D80000
7	0DC0000

On-Board Addressing

Only a small number of addresses are decoded for on-board functions. These addresses are not fully decoded in hardware. Undefined addresses should not be used; they may affect on-board functions. Reads and writes are always full words, even if only 8-bit values are significant.

Interface Registers and Command Descriptions

The following paragraphs list the registers used in Ethernet interface operations and the command descriptions that select the I/O functions.

ID Register (Base Address 03FFFF - 03FFC0)

When the UNIX PC is first powered up, the UNIX kernel reads the ID register into memory. The ID register is a set of 8-bit registers located at odd byte addresses in the upper 32 words of the board address block. The upper four words contain the required board identification numbers. The lowest six words contain the board-specific Ethernet station address. The appropriate driver must determine where the hardware is located. The getslot system call (see UNIX System V User's Manual, drivers(7)) locates the offset (slot). The base address is then added to the offset address to access the appropriate registers.

Base Address	R/W	Description
03FFFF	R	MSB of ID, two's complement
03FFFE	R	Not Used
03FFFD	R	LSB of ID less than two's complement
03FFFC	R	Not Used
03FFFB	R	MSB of ID
03FFFA	R	
	through	
03FFCD		Not Used
03FFCC	R	MSB Ethernet Address
03FFCA	R	Not Used
03FFC9	R	Ethernet Address
03FFC8	R	Not Used
03FFC7	R	Ethernet Address
03FFC6	R	Not Used
03FFC5	R	Ethernet Address
03FFC4	R	Not Used
03FFC3	R	Ethernet Address
03FFC2	R	Not Used
03FFC1	R	LSB Ethernet Address
03FFC0	R	Not Used

Software Reset

A write to any of the four board ID addresses causes the board to be reset and put into an inactive state.

Base Address	R/W	Description
03FFFF	W	Software Reset
	through	
03FFF8	W	Software Reset

LANCE Data Latch

This read-only, 16-bit latch is required to accommodate the slow LANCE register access time to the expansion-board timing requirements through a two-step process. Reading the on-chip LANCE registers does not produce valid data in time for the active I/O cycle, but the data is stored in the LANCE data latch. Subsequently, a read of the latch will return the desired data to the CPU.

Base Address	R/W	Description
000006	R	LANCE Data Latch

Status Ring Address

This write-only, 16-bit register is used to supply bits A9 to A21 of the status ring address. Bits A1 to A8 are supplied by an on-board counter which is cleared on reset. Together, they supply the addressing for the on-board DMA to place LANCE status in memory automatically. A write to this address clears any pending interrupts.

Base Address	R/W	Description
000006	W	Status Ring Address

Control Register

The board contains a read/write, 4-bit control register to provide selection of interrupt line, LAN interface type, and a DMA disable for diagnostic purposes. This register is reset to zeros by hardware or software reset.

Bit	Signal	Description
D0	DMAEN	1 = DMA Enabled 0 = DMA Disabled
D1	RESERVED	1 = Other Selected 0 = Ethernet Selected
D2	INTSEL	1 = Use Interrupt 01 0 = Use Interrupt 05
D3	SPARE	

A read of this address also resets the board interrupt.

Base Address	R/W	Description
000004	RW	Control Register

LANCE Register Address and Data Ports

The LANCE chip in slave mode contains two ports. The register address port is a 2-bit port that selects which of the four 16-bit control and status ports are accessed through the register data port.

Base Address	R/W	Description
000002	RW	LANCE Register Address Port
000000	RW	LANCE Register Data Port

Software Operation

Once the LANCE chip has been started, all data and status transfers are done through DMA. No I/O access is permitted to the board except the software reset and interrupt reset functions.

Troubleshooting

The following procedures are a simplified description for troubleshooting a UNIX PC Ethernet Expansion Board that is not functioning properly or has failed a diagnostics test. The following items are required to perform these procedures:

- Kernel debugger program
- An Oscilloscope
- Voltmeter (VOM)
- Logic Analyzer

The following reference books will also be useful:

- Ethernet Board Installation and Diagnostics Guide
- Advanced Micro Devices Local Area Network Controller AM7990 (LANCE) Technical Manual

Before beginning with the troubleshooting procedures, check the schematic against the ICs on the board so they can be identified readily. Also, during operation of the expansion board, the voltage at J2-13 should be 12 - 13 Vdc.

Troubleshooting is concerned with the EEB's three basic cycles and how they relate to components that have failed. Figure 2 is a diagram of the Ethernet states and Table 3 lists the state assignment functions during specific cycles. These cycles are:

- I/O cycle
- DMA cycle
- Interrupt cycle

I/O Cycle

The I/O cycle consists of three individual cycles as follows:

- Register Read/Write cycle
- Board ID Read-Only cycle
- CPU LANCE Read/Write cycle

When the EEB has been reset either by a hardware or software reset, it is at the idle state. By using the Kernel debugger program, the I/O cycle can be examined for the three read and write functions listed above. A failure of any of these cycles indicates the following hardware problems:

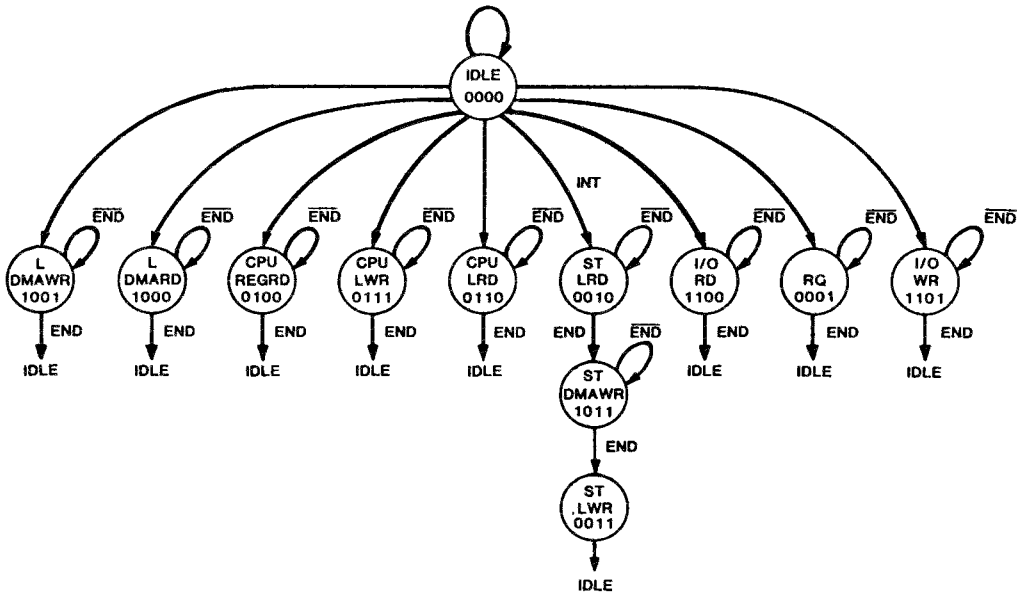


Figure 2 Ethernet State Diagram

Table 3 State Assignments

Cycle				Function
3	2	1	0	
0	0	0	0	IDLE
0	0	0	1	
0	0	1	0	STLRD
0	0	1	1	STLWR
0	1	0	0	CPUREGRD
0	1	0	1	
0	1	1	0	CPULRD
0	1	1	1	CPULWR
1	0	0	0	LDMARD
1	0	0	1	LDMAWR
1	0	1	0	
1	0	1	1	STDMAWR
1	1	0	0	IORDCYC
1	1	0	1	IOWRCYC
0	0	0	1	RQCYC
1	1	1	1	

Register Read/Write Cycle

A failure of this cycle is a result of a malfunctioning PAL or wrong PAL equation, a cycle status being misread to the state machine, or a clock failure. The following components should be checked for the listed conditions:

- 4B (PAL16L8A located on schematic page 4) is either malfunctioning or the wrong equation is being read.
- 4C (PAL20R8A located on schematic page 5) is either malfunctioning or the wrong equation is being read. Also, use the logic analyzer to check pins 19 - 22 for the correct CYC0* - CYC3* sequence (refer to the cycle diagram, Figure 3).
- 4C - 4F (PAL20R8A, PAL16R8A, PAL16R6A, and PAL16R8A located on schematic sheet 5) are not receiving clock signals on pin 1.

Board ID Read-Only Cycle

The following components should be checked for failure:

- 2F (PROM 74S288 or 823123 located on schematic sheet 4) has failed.
- 4B (PAL16L8A located on schematic sheet 4) has failed.
- There is no clock present.

CPU LANCE Read/Write Cycle

The LANCE location address is being accessed by writing to the Register Address Pointer (RAP). The CPU LANCE Read cycle is performed in two steps. First, location 0000 is read; second, location 0006 is read-returning the valid data from the address pointed to by RAP.

If the CPU LANCE Read/Write cycle fails, check the following components for the listed conditions:

- 4C (PAL20R8 located on schematic sheet 5) the pin 19 - 22, CYC0* - CYC3* is not correct.
- 4E (PAL16R6A located on schematic sheet 5) is not providing the proper signal interface (DAS* and READY*) to the LANCE.
- 4H (AM 7990 LANCE located on schematic sheet 3) is malfunctioning.

DMA Cycle

The DMA cycle consists of three individual cycles as follows:

- DMA Read (single or burst) cycle
- DMA Write (single or burst) cycle
- STATUS DMA Write (single) cycle

A failure of any of these cycles indicates the following hardware problems as discussed in the following paragraphs.

DMA Read/Write (Single)

On the first two cycles, DMA Read and DMA Write, the address is provided by LANCE. For STATUS DMA Write, the address comes from the on board registers 1G and 1E, and ring counters 2B and 2C, located on schematic page 4. These are written to during initialization.

The LANCE performs 12 single DMA READ cycles when a 1 is being written to the initializing bit of the LANCE control-status register. Using a logic analyzer, check 5D, pin 8 (RQ) located on schematic page 4, for these 12 requests corresponding to bus grant (BG) from 1H, pin 16 with 1A pin 12 (XR/W*) high.

Also, check the signal timing at LANCE as follows:

- 4H pin 17 (HOLD*) schematic page 3
- 4H pin 19 (HLDA*)
- 4H pin 18 (LAS*)
- 4H pin 14 (DAS*)
- 4H pin 22 (READY*)

Refer to the timing diagram in Figure 3.

After initialization, LANCE generates the interrupt active low at 4H pin 11. The state machine gets the status from the LANCE and writes to the status ring. The content is 01C1 (see the bit definition in the LANCE technical manual). The state machine then generates the interrupt to the CPU at the same time that it writes 1s to the LANCE, clearing the LANCE interrupt and status. If the initialization is complete and correct, the status content at the CPU memory will be 01C1.

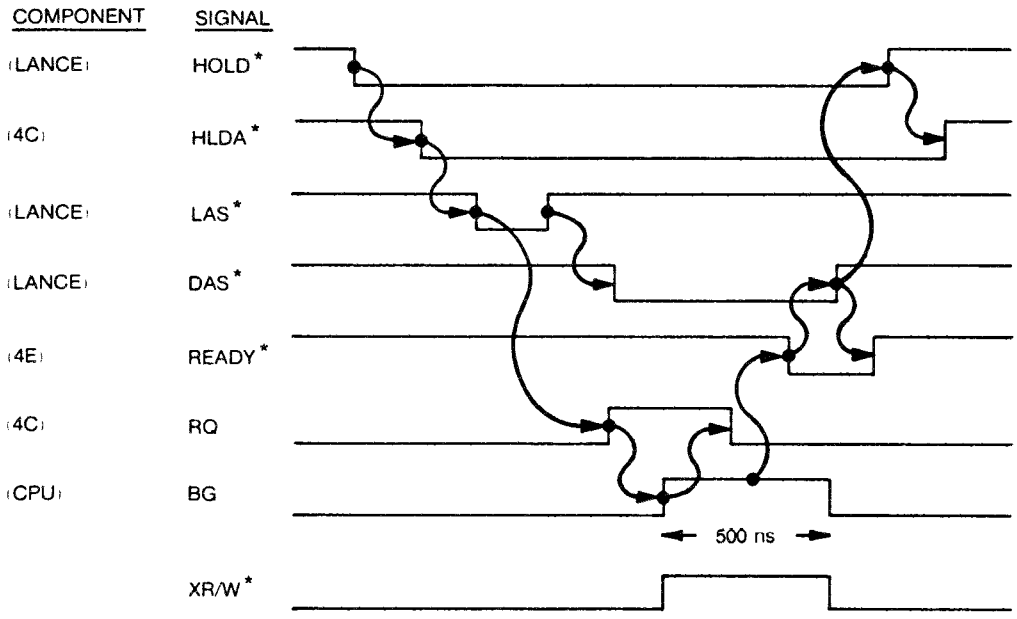


Figure 3 Expansion Board Cycle Diagram

Next, the LANCE performs a single DMA read to the TMD1 every 1.6 msec. Using the oscilloscope, check the RQ and BG activity. BG should have a 500 nsec pulse width. RQ should be gone 100 nsec after BG is active. If there is no activity (neither RQ nor BG) check if HOLD*, HLDA*, LAS*, DAS*, READY*, and CYC0 through CYC3* are generated from 4C, located on schematic page 5.

The cycle should not be stuck at DMA Read longer than 3 us. If it is, this indicates that 4C and 4E on schematic page 5 or the LANCE is defective.

DMA Read/Write (Burst)

Using a logic analyzer, observe the DMA Read/Write burst. The burst should consist of a transfer of 8 words, except for the last cycle if data is fewer than 8 words. If the DMA Read/Write burst does not perform properly, check 4C and 4E on schematic page 5, or the LANCE.

Interrupt Cycle

The interrupt cycle consists of the LANCE sending an interrupt to the state machine at the completion of an operation. If there is an error, the state machine reads the LANCE status and requests that the status DMA Write cycle be performed. Once the state machine gets the bus, it writes to the location of the current status ring address and updates the status ring address. Then the state machine generates the interrupt to the CPU. Note that the status ring content normally shows whether the problem is in either reception or transmission of data. Check the receive or transmit descriptor ring for further status information.

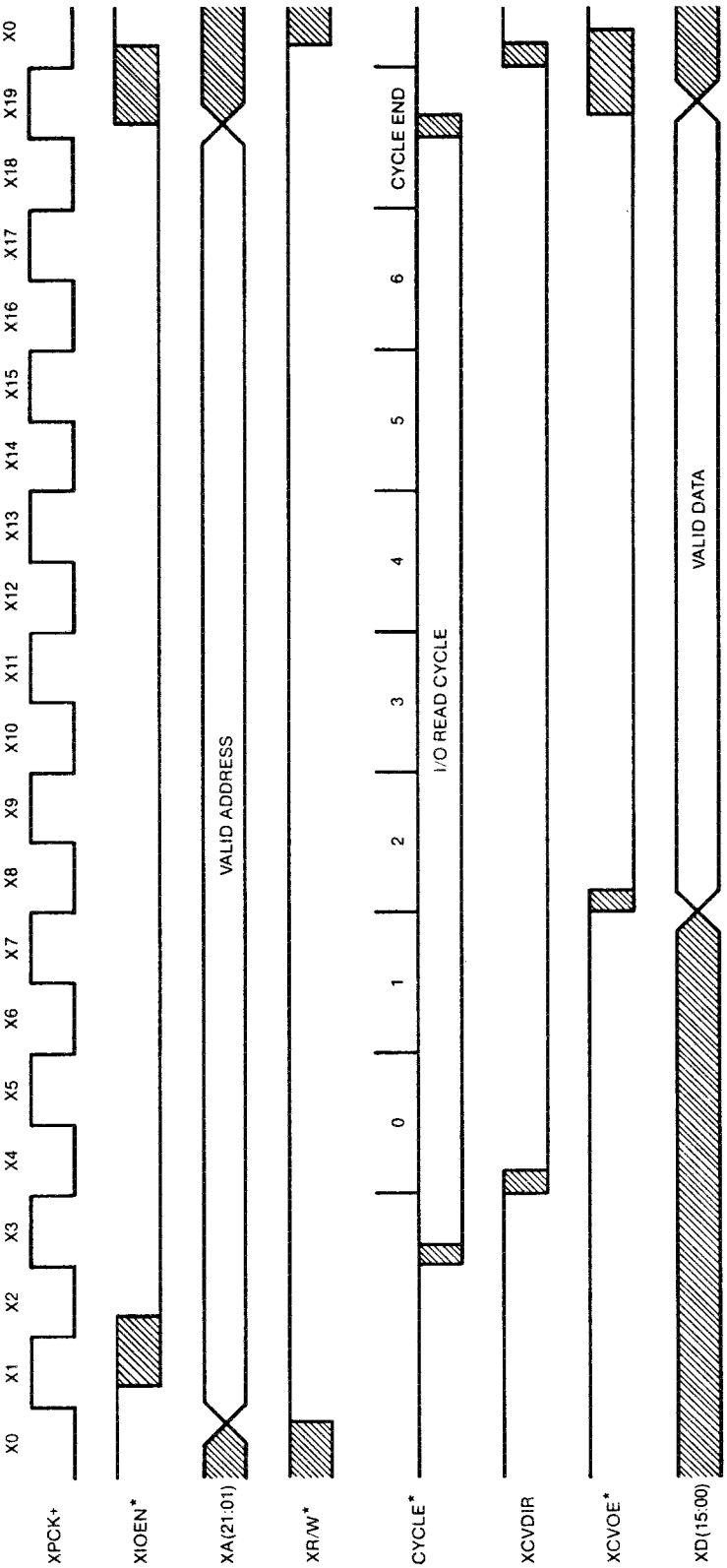


Figure 4 CPU non-LANCE Read-Timing Diagram

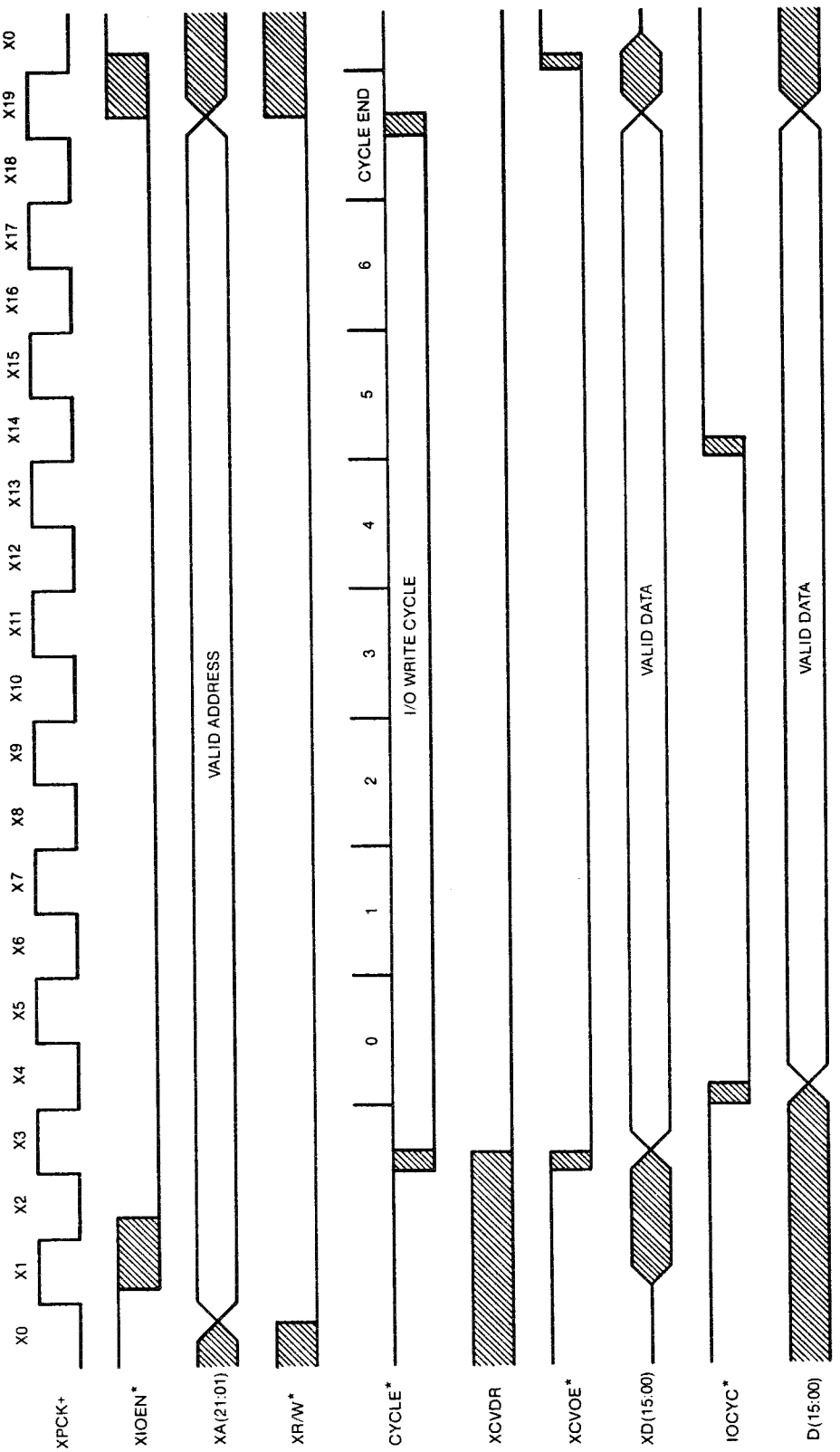


Figure 5 CPU non-LANCE Write-Timing Diagram

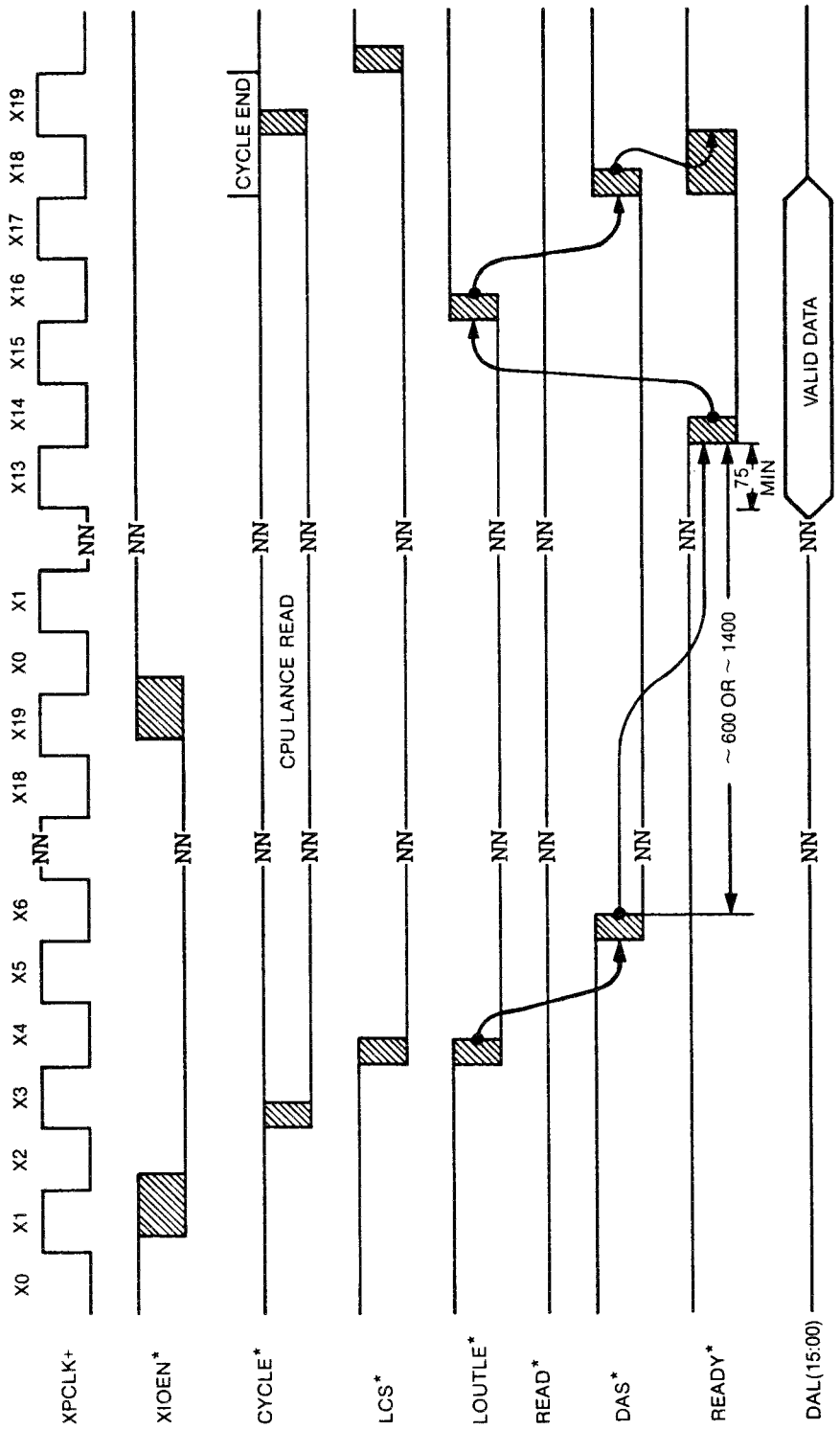


Figure 6 CPU LANCE Read-Timing Diagram

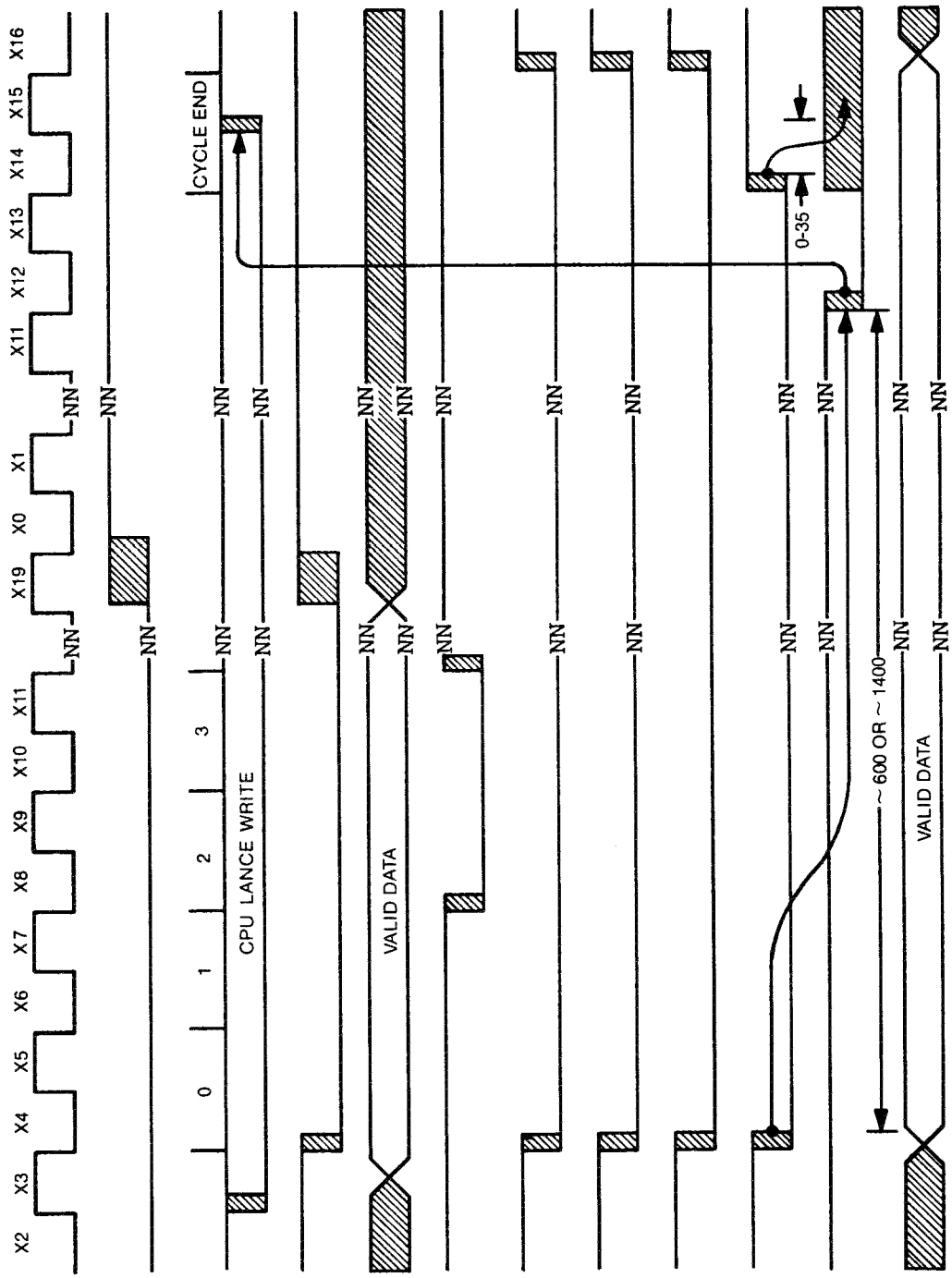


Figure 7 CPU LANCE Write-Timing Diagram

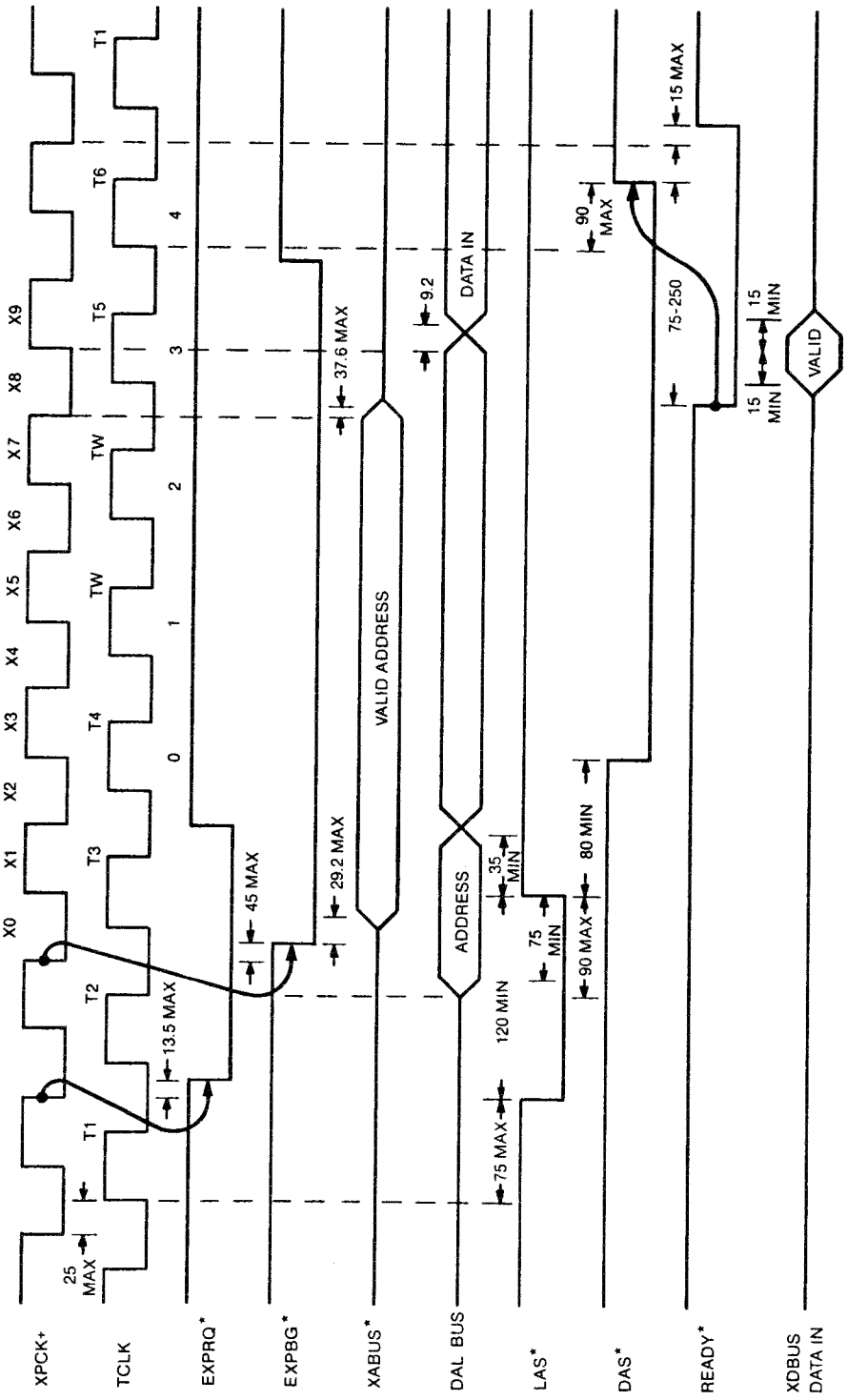


Figure 8 LANCE DMA Read Cycle

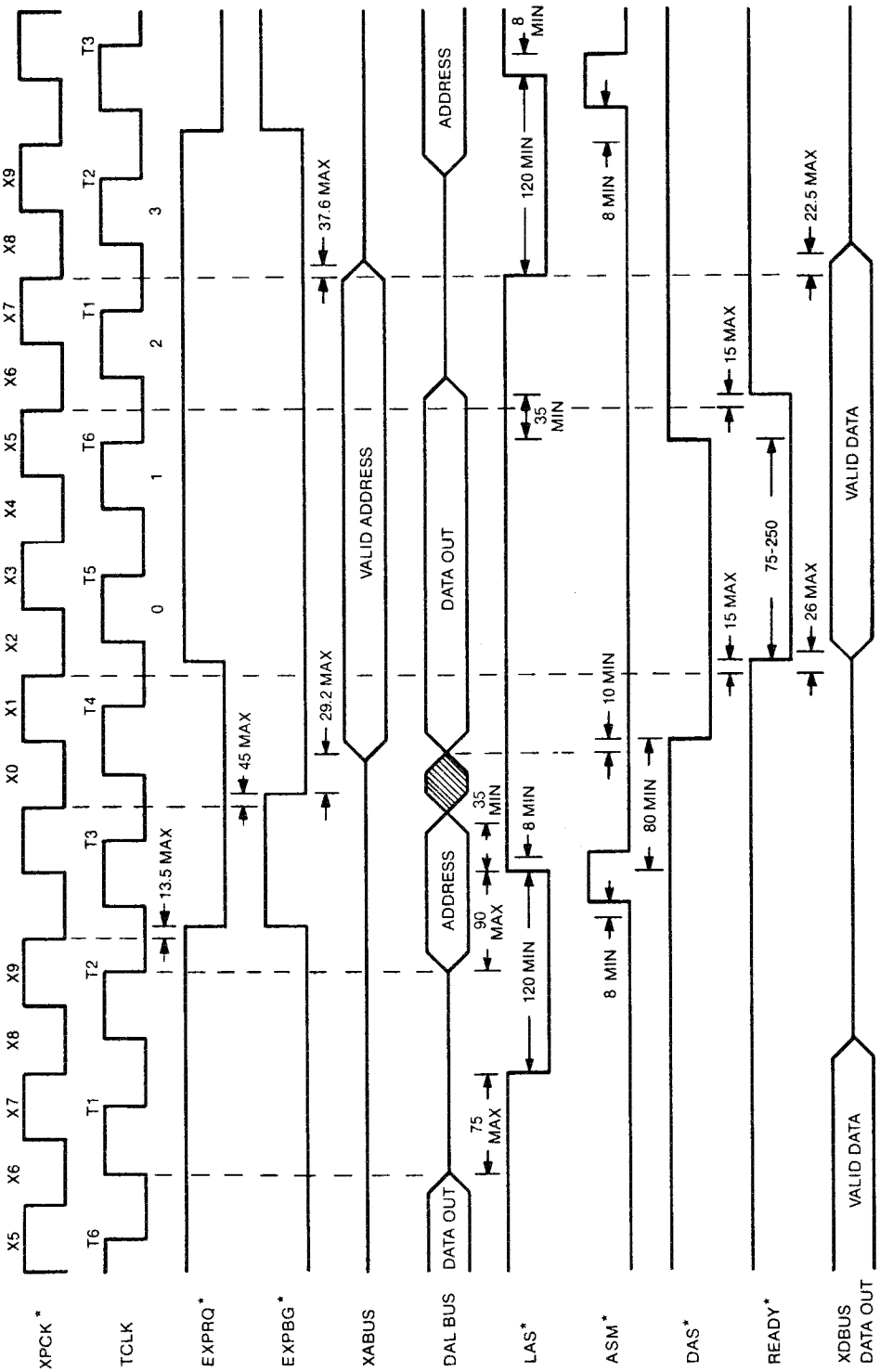
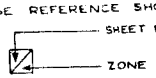


Figure 9 LANCE DMA Write Cycle

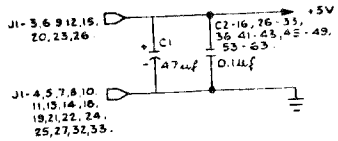
REVISIONS					
ZONE	REV	DESCRIPTION	DATE	CHK	APPROVED
	A	RELEASE TO CONTROL			

NOTES: UNLESS OTHERWISE SPECIFIED.

1. ALL RESISTOR VALUES ARE IN OHMS, 1/4W.
2. ALL CAPACITOR VALUES ARE IN MICROFARADS.
3. PAGE REFERENCE SHOWN AS

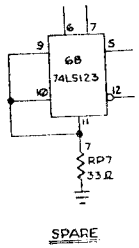


4. THE FOLLOWING COMPONENTS ARE NOT USED ON PCB
C37-40, K1-2, R10, VR2, CR2, SPR1.



I.C. VOLTAGE CHART

DEVICE	REF. DESGN.	VCC	GND	PAGE NO.	UNUSED GATES
74F04	5B, 3C, 6A	14	7	2,4,5,3	5B 12, 6A (6 8 10 12)
74F08	6H	14	7	2,5	
74F64	6D	14	7	2	
74F74	2A, 5A, 5D, 6C	14	7	2,4,5	6C (1-6)
74F20	6E	14	7	2,3	6E (6,11)
74F240	1H	20	10	4	
74F244	1A, 2C, 1F	20	10	4,2	
74F245	1C, 1D	20	10	4	
74F373	2D 2G, 3D, 3E, 3F, 3G, 3H	20	10	2	
74F374	1E, 1G	20	10	4	
74LS74	5C	14	7	5	
74LS123	6B	16	8	5	
74LS125	5E	14	7	5	
74LS161	4A	16	8	5	
74LS175	3B	16	8	4	
74LS244	2H	20	10	2	
74LS393	2B, 5F	14	7	4,5	5F (8-13)
74S38	3A	14	7	5	
74S35	1B	16	8	4	
74S288	2F	16	8	4	
75453	7F	8	4	3	
PAL16R6A	4E	20	10	5	
PAL16R8A	4D4F	20	10	5	
PAL20R8A	4C	24	12	5	
PAL16L8A	4B	20	10	4	
XFMR ISO.	8G			3	
AM7990	4H	48	1,24	3	
AM7992	6G	18,19	6,7,15	3	
DELAY LINE	6F	14	7	3	



SPARE

REFERENCE DESIGNATIONS	
LAST USED	NOT USED
C63	
CR2	
E9	
F1	
K2	
L1	
R13	
RP8	
VR2	

SPARES (EXCL. I.C.'S)	
PART	UNUSED PINS
RP4	4,7
RP7	6
J1	1, 31, 34, 36, 37, 42-45, 67, 71-74, 83-91
J2	4,7,8,11,14,15

QTY PER CAR	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION			MATERIAL SPECIFICATION
		PARTS LIST			

INCHES

THIRD ANGLE PROJECTION

NEXT ASSY | USED ON

APPLICATION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCES ARE: .xx ±.01, .xxx ±.005, ANGLES ±1°

MATERIAL

FINISH

DO NOT SCALE DRAWING

APPROVALS	DATE
Drawn H.NGUYEN	11-21-85
CHECKED	
APPD	

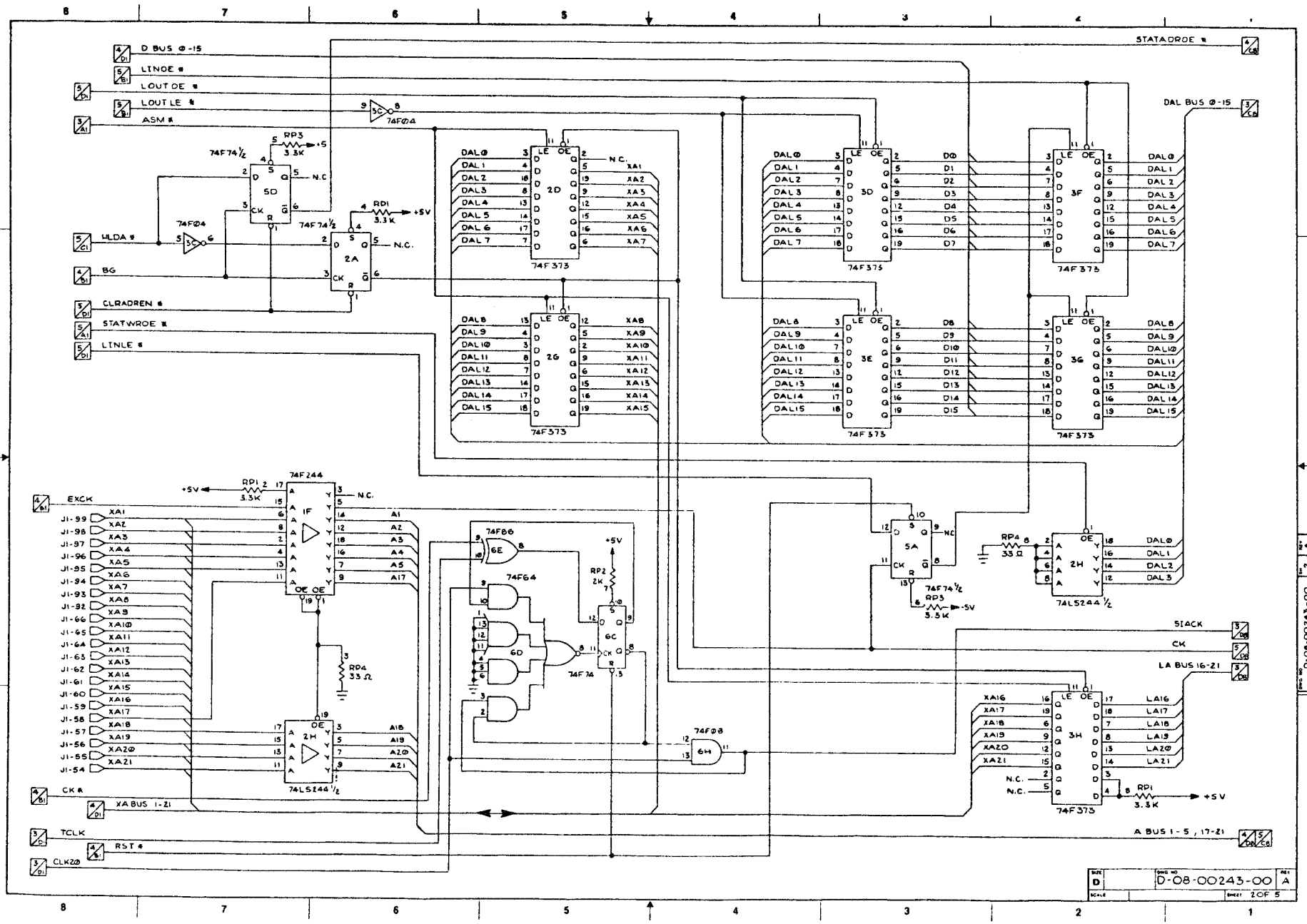
Convergent Technologies™

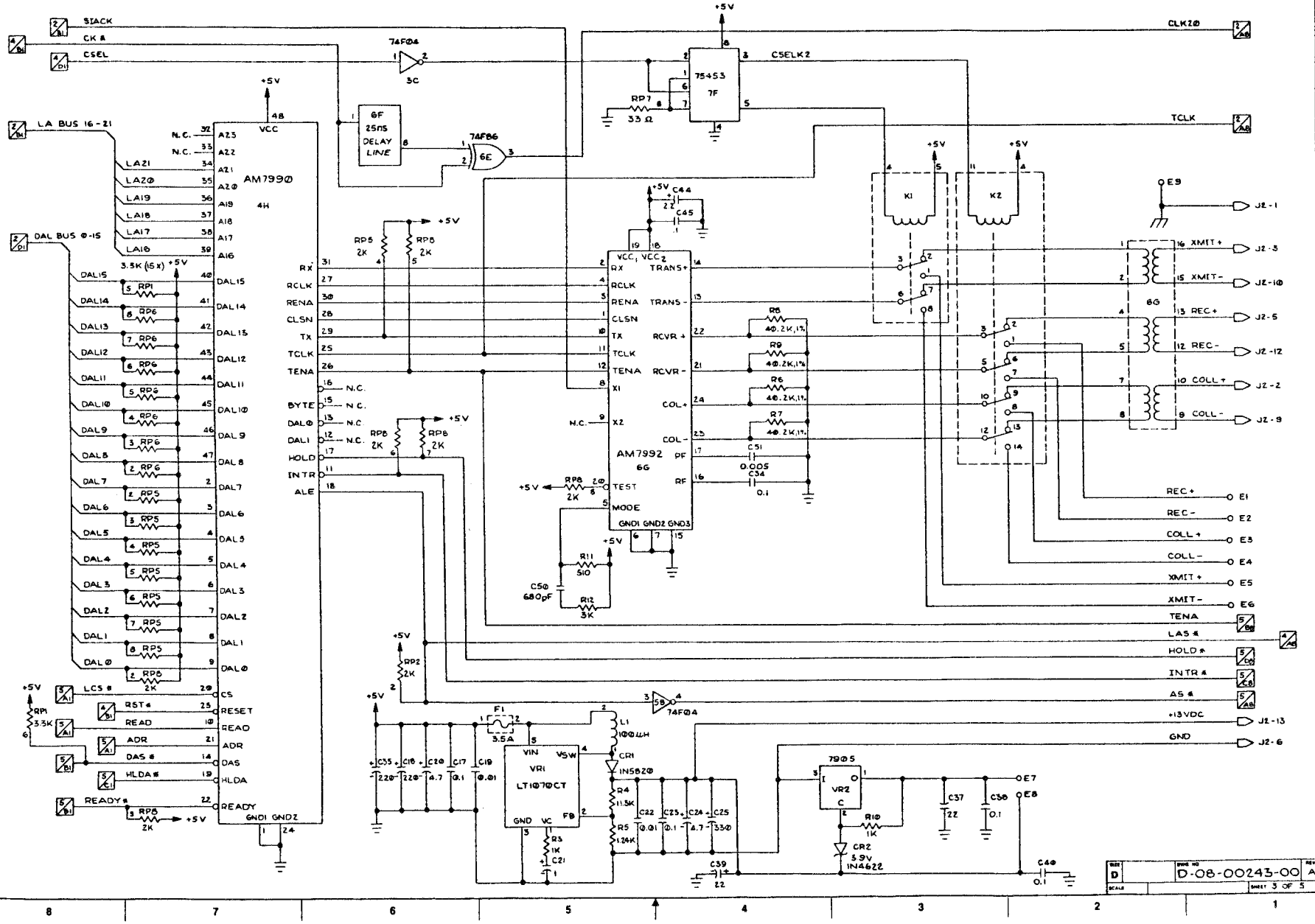
TITLE: SCHEMATIC, ETHERNET

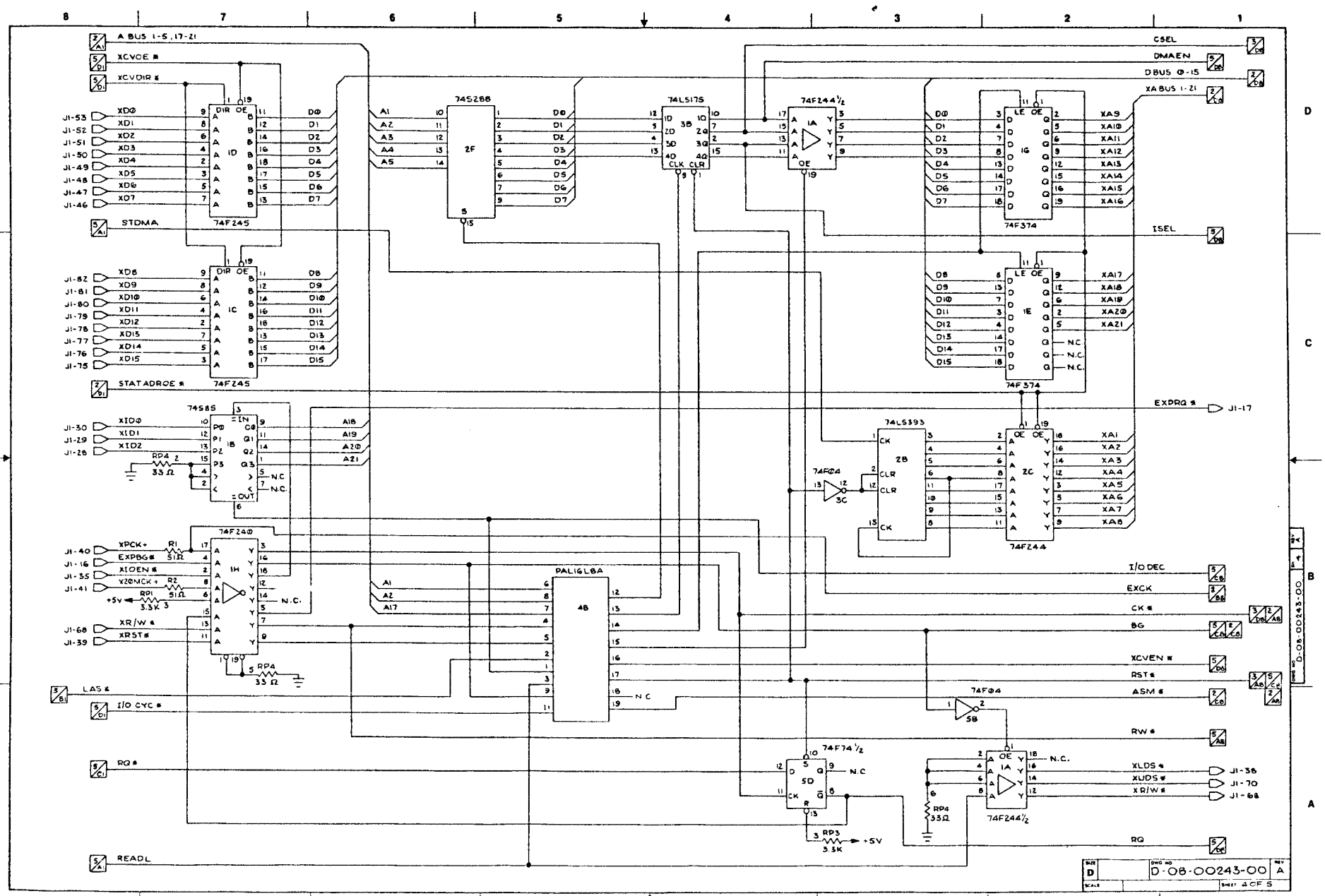
SIZE D | DWG NO. D-08-00243-00 | REV A

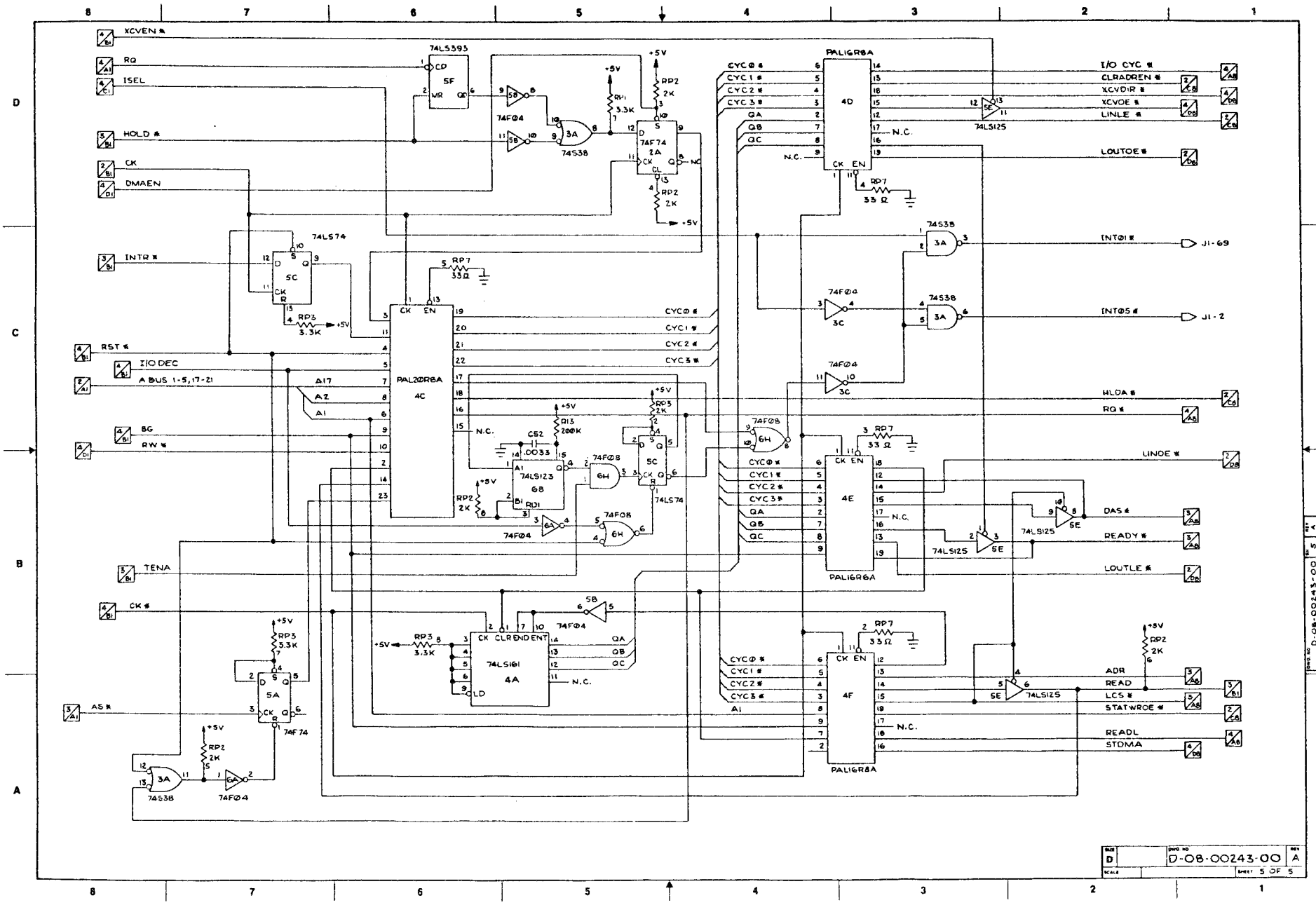
SCALE — | SHEET 1 OF 5

D-08-00243-00 REV A


D BUS Ø-15
LINOE #
LOUT OE #
LOUT LE #
ASM #
ULDA #
BG
CLRADREN #
STATWROE #
LINLE #
EXCK
CK #
XABUS 1-21
TCLK
RST #
CLK2Ø
STATADROE #
DAL BUS Ø-15
SIACK
CK
LA BUS 16-21
A BUS 1-5, 17-21
74F74½
74FØ4
74FØA
74F373
74F244
74LS244½
74FØ8
74F86
74F64
74F74
RP1 3.3K
RP2 2K
RP3 3.3K
RP4 33Ω
+5V
-5V
N.C.
1D
2D
2A
2G
3D
3E
3F
3G
5A
6C
6D
6E
6H
1F
2H
3H


SIACK
CK 8
CSEL
74F04
5C
+5V
CLK20
CSELK2
75453
7F
RP7
33 Ω
TCLK
LA BUS 16-21
DAL BUS 0-15
AM7990
4H
VCC
LA23
LA22
LA21
LA20
LA19
LA18
LA17
LA16
DAL15
DAL14
DAL13
DAL12
DAL11
DAL10
DAL9
DAL8
DAL7
DAL6
DAL5
DAL4
DAL3
DAL2
DAL1
DAL0
RX
RCLK
RENA
CLSN
TX
TCLK
TENA
BYTE
DAL0
DAL1
HOLD
INTR
ALE
CS
RESET
READ
ADR
DAS
HLDA
READY
GND1 GND2
6F
25ns
DELAY
LINE
74F86
6E
3.5K (15x)
RP1
RP5
RP6
2K
RP8
20
510
5K
680pF
C50
C51
0.005
C54
0.1
C44
22
C45
1
AM7992
6G
VCC1 VCC2
RX
RCLK
RENA
CLSN
TX
TCLK
TENA
XI
XZ
TEST
MODE
GND1 GND2 GND3
TRANS+
TRANS-
RCVR+
RCVR-
COL+
COL-
PF
RF
R6
R9
R7
40.2K,1%
K1
K2
6G
E9
J2-1
J2-3
J2-10
J2-5
J2-12
J2-2
J2-9
16 XMIT+
15 XMIT-
13 REC+
12 REC-
10 COLL+
9 COLL-
REC+
REC-
COLL+
COLL-
XMIT+
XMIT-
TENA
LAS 8
HOLD 8
INTR 8
AS 8
+13VDC
GND
E1
E2
E3
E4
E5
E6
RP2
74F04
F1
3.5A
L1
100μH
CR1
IN5820
VIN
VSW
VR1
LT1070CT
GND
VC
FB
R4
11.5K
R5
1.24K
R3
1K
C21
1
C55
220
C16
220
C20
4.7
C17
0.1
C19
0.01
C22
0.01
C23
0.1
C24
4.7
C25
330
C39
22
7905
VR2
R10
1K
CR2
5.9V
IN4622
C37
22
C36
0.1
C40
0.1
E7
E8
D-08-00243-00
A
SHEET 3 OF 5

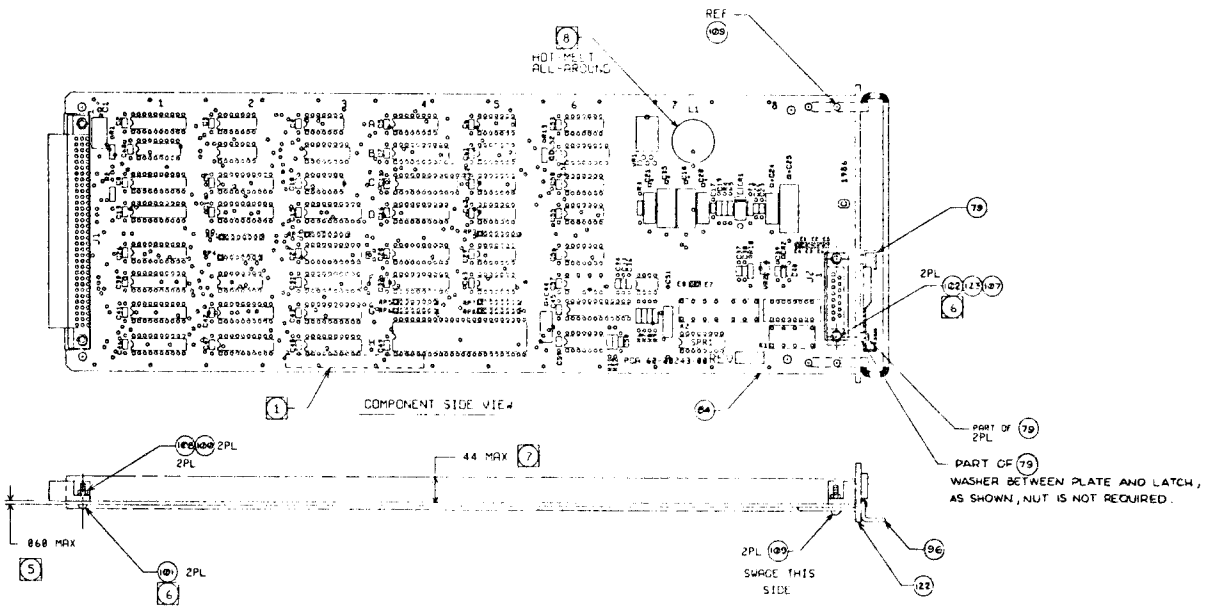

A BUS 1-5, 17-21
XCVOE #
XCVDIR #
XD0
XD1
XD2
XD3
XD4
XD5
XD6
XD7
J1-53
J1-52
J1-51
J1-50
J1-49
J1-48
J1-47
J1-46
74F245
STDMA
XD8
XD9
XD10
XD11
XD12
XD13
XD14
XD15
J1-82
J1-81
J1-80
J1-79
J1-78
J1-77
J1-76
J1-75
STATADROE #
74S288
74LS175
74F244½
74F374
CSEL
DMAEN
DBUS 0-15
XABUS 1-21
ISEL
XA9
XA10
XA11
XA12
XA13
XA14
XA15
XA16
XA17
XA18
XA19
XA20
XA21
74S85
XID0
XID1
XID2
J1-30
J1-29
J1-28
RP4
33 Ω
A18
A19
A20
A21
74F240
XPCK+
EXPBG #
XIOEN #
XA0MCK+
XR/W #
XRST #
J1-40
J1-16
J1-35
J1-41
J1-68
J1-39
R1
R2
RP1
5 kΩ
3.3K
PAL16L8A
74LS393
74F04
74F244
EXPRQ #
J1-17
I/O DEC
EXCK
CK #
BG
XCVEN #
RST #
ASM #
RW #
XLDS #
XUDS #
XR/W #
J1-36
J1-70
J1-68
74F74½
RP3
+5V
LAS #
I/O CYC #
RQ #
READL
RQ
D-08-00243-00
A
SHEET 4 OF 5


XCVEN *
RQ
ISEL
HOLD *
CK
DMAEN
INTR *
RST *
I/O DEC
A BUS 1-5,17-21
BG
RW *
TENA
CK *
AS *
74LS393
74LS74
74F04
74S38
74F74
PAL20R8A
74LS123
74LS161
74LS125
PALIGR8A
+5V
RP7 33Ω
RP3 3.3K
RP2 2K
RP1 3.3K
R13 200K
C52 .0033
CYC0 *
CYC1 *
CYC2 *
CYC3 *
I/O CYC *
CLRADREN *
XCVDIR *
XCVOE *
LINLE *
LOUTOE *
INT01 *
INT05 *
HLDA *
RQ *
LINOE *
DAS *
READY *
LOUTLE *
ADR
READ
LCS *
STATWROE *
READL
STDMA
J1-69
J1-2
N.C.
D-08-00243-00
SHEET 5 OF 5

REVISIONS					
ZONE	REV	DESCRIPTION	DATE	CHK	APPROVED
	A	RELEASE TO CONTROL AC PER ECS #E5 3			

NOTES: UNLESS OTHERWISE SPECIFIED

1. MARK APPROPRIATE DATE (BAR) CODE TO SHOW DATE OF MANUFACTURE
2.
3. FOR COMPLETE LIST OF MATERIALS SEE D-60-00243-00
4. SCHEMATIC REF D-00-00243-00.
5. ON SOLDER SIDE ALL COMPONENT LEADS MUST BE CUT TO A LENGTH NOT EXCEEDING I.C. LEAD PROTRUSION OF MIN .030 AND MAX .060 (TYP .030)
6. CONNECTOR MOUNTING SCREW IS INSERTED FROM SOLDER SIDE OF BOARD
7. COMPONENT HEIGHT SHALL NOT EXCEED .440.
8. AFFIX INDICATED COMPONENTS TO P.C.B. USING HOT-MELT ADHESIVE, AFTER WAVE-SOLDER.
9. THE FOLLOWING COMPONENTS ARE NOT USED ON THIS VERSION:
   C37-40 CR2
   K1, 2 SPR1
   R10
   VR2



INCHES					
THIRD ANGLE PROJECTION					
	S-4				
NEXT ASSY	USED ON				
APPLICATION					

PARTS LIST

QTY REQD	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION	MATERIAL SPECIFICATION

DO NOT SCALE DRAWING

MATERIAL
FINISH

APPROVALS	DATE
DRAWN D. Sitnick	84/25/8
CHECKED	
APVD	

Convergent Technologies™

TITLE: ASSEMBLY DRAWING, ETHERNET P.C.B.

SIZE	DWG NO	REV
D	D-60-00243-00	A

SCALE 1/1 SHEET 1 OF 1

D-60-00243-00 REV A

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	CHK	APPROVED
	A	RELEASE TO CONTROL			

NOTES:

DO NOT SCALE THIS DRAWING

UL SYMBOL REQUIRED

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

MECHANICAL TOLERANCE XX +/- .010 XXX +/- .005

FRONT TO BACK REGISTRATION +/- .003

MINIMUIM CONDUCTOR WIDTH .008

MINIMUM AIRGAP .008

MATERIAL TO BE GLASS EXPOXY TYPE FR-4, UL APPROVED
1 OZ COPPER PLATE TO 2 OZ ON OUTER LAYERS PER
MIL-P-47226, MIN 99.5 % PURE. COLOR NATURAL.

METAL-CLAD LAMINATES SHALL BE IN ACCORDANCE WITH MIL-P-13949

BOARD THICKNESS TO BE .062 +/- .005 (GLASS TO GLASS)

INSPECTION CRITERIA PER IPC-A-600C

VENDOR SHALL SELECT PROCESSES, EQUIPMENT AND MATERIALS
IN ORDER TO ACHIEVE ZERO DEFECT PRODUCT

SOLDERMASK BOTH SIDES OF BOARD USING ARTWORK PROVIDED
SOLDERMASK SHALL BE PC401, DRY FILM OR PROBIMER

SILKSCREEN COMPONENT SIDE USING ARTWORK PROVIDED
COLOR: WHITE, NON-CONDUCTIVE

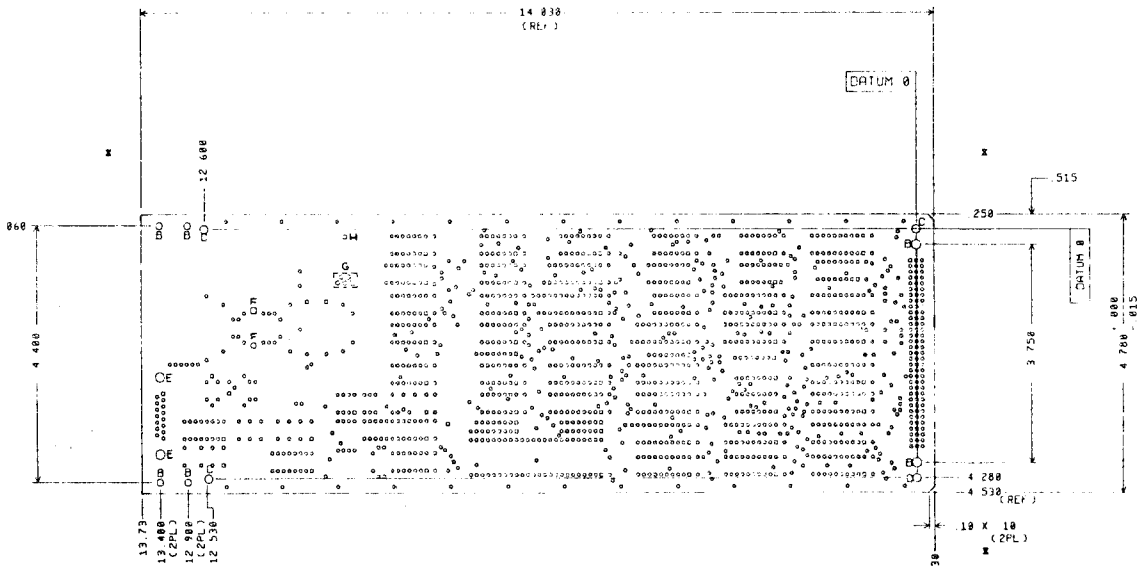
UNLESS OTHERWISE SPECIFIED ALL HOLES ARE PLATED THROUGH

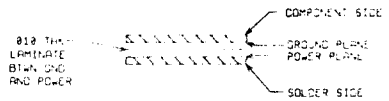
ALL HOLES TO BE FINISHED SIZE AFTER PLATING

ALL HOLES SHALL BE LOCATED WITHIN .003 OF THEIR
TRUE POSITION WITH RESPECT TO THE PAD CENTER

HOLE SCHEDULE

CODE	DESCRIPTION	QTY	PLATING
UNMKD	.039 ± .003	A/R	YES
B	.093 ± .003	6	YES
C	.125 ± .003 .002	4	NO
E	.128 ± .003	2	YES
F	.055 ± .003	2	YES
G	.062 ± .003	5	YES
H	.152 ± .003	1	YES





LAYER ORIENTATION

(NOT TO SCALE)

PARTS LIST			
QTY PER DWG	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION	MATERIAL SPECIFICATION

INCHES

THIRD ANGLE PROJECTION

NEXT ASSY | USED ON

APPLICATION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE
.XX ±.010
.XXX ±.005
ANGLES ±1°

MATERIAL

FINISH

DO NOT SCALE DRAWING

APPROVALS | DATE

DRAWN W NGUYEN 4-25-86

CHECKED

QA

MFG

Convergent Technologies™

TITLE: FABRICATION DWG, ETHERNET

SIZE D | DWG NO D-43-00243-00 | REV A

SCALE 1:1 | SHEET 1 OF 1

D-43-00243-00